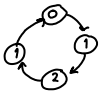
Lecture 22 : CS

Thursday, September 3rd, 2009
8:34 AM

Sequential-Logic-Circuit Design Technique

We will focus on synchronous design.

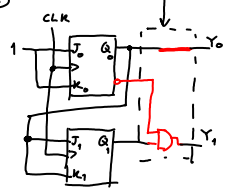
All FFs are clocked by the same CLK signal.



Current state $Q_1 Q_0$	Next state $Q_1 Q_0$
0 0	0 1
0 1	1 0
1 0	0 0
1 1	

$Y_1 = Q_1 \overline{Q}_0$

Input $Q_1 Q_0$	Output $Y_1 Y_0$
0 0	0 0
0 1	0 1
1 0	1 0
1 1	0 1

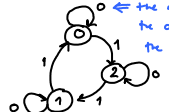


Let's try to work on the same problem as last time

However, we will add "CTEN" input.

⇓

New state diagram



← the number on the arrow indicate the value of CTEN.

D-FF version

Recall : without the CTEN

$$D_1 = \overline{Q}_1 \overline{Q}_0$$
$$D_0 = Q_1$$

We know that when CTEN = 1

D_1 = same.

D_0 =

When CTEN = 0

$$D_1 = Q_1$$
$$D_0 = Q_0$$

Combine the two cases :

$$D_1 = CTEN \cdot \overline{Q}_1 \overline{Q}_0 + \overline{CTEN} \cdot Q_1$$
$$D_0 = CTEN \cdot Q_1 + \overline{CTEN} \cdot Q_0$$

J-K FF versio

When CTEN

$J_1 = \overline{Q}_1$

$K_1 = 1$

$J_0 = Q$

$K_0 = 1$

⇓

Combine versi

$J_1 = CTEN \cdot$

$K_1 = CTEN$

$J_0 = CTEN \cdot$

$K_0 = CTEN$

n

$= 1$

When CTEN = 0

$J_1 = 0$

$K_1 = 0$

$J_0 = 0$

$K_0 = 0$

on

$\cdot \overline{Q_0} + \overline{CTEN} \cdot 0$

$\cdot Q_1$